

Docket No.: 202009US-2 DIV

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF

Shigenobu MAEDA : EXAMINER:

SERIAL NO: NEW APPLICATION

FILED: HEREWITH : GROUP ART UNIT:

FOR: MANUFACTURING METHOD OF  
SEMICONDUCTOR WAFER,  
SEMICONDUCTOR MANUFACTURING  
APPARATUS, AND SEMICONDUCTOR  
DEVICE

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS  
WASHINGTON, D.C. 20231

SIR:

Prior to examination on the merits, please amend the above-identified patent  
application as follows:

IN THE CLAIMS

Please cancel without prejudice or disclaimer Claims 1-20.

Please add Claims 21-24 as follows:

--21. A method of manufacturing a semiconductor device for building a circuit composed  
of combined plural circuit elements into a semiconductor chip, comprising:

expressing a layout pattern of said circuit by using mask patterns respectively prepared  
for said plural circuit elements.

22. The method of manufacturing a semiconductor device according to Claim 21,  
wherein

each of said mask patterns respectively prepared for said plural circuit elements has a mark for positioning, and

positioning of said mask patterns is performed by superposing one of said marks on another of said marks.

23. A semiconductor device manufactured by the method according to Claim 21.

24. A semiconductor device manufactured by the method according to Claim 22.--

#### REMARKS

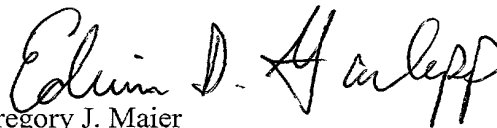
Favorable consideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-20 canceled, and Claims 21-24 added by way of the present preliminary amendment. Claims 21-24 correspond to non-elected claims 51-54 of the parent application and therefore addition of these claims is not believed to raise a question of new matter.

Accordingly, examination in the merits is believed to be in order and an early and favorable action is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,  
MAIER & NEUSTADT, P.C.



Gregory J. Maier  
Registration No. 25,599  
Attorney of Record  
Edwin D. Garlepp  
Registration No. 45,330



**22850**

Tel. No.(703) 413-3000

Fax #: (703)413-2220

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